HORIZON EUROPE PROGRAMME

TOPIC HORIZON-CL5-2021-D3-03

Demonstration pilot lines for alternative and innovative PV technologies

(Novel c-Si tandem, thin film tandem, bifacial, CPV, etc.)

GA No. 101084046

Digitalised pilot lines for silicon heterojunction tunnel interdigitated back contact solar cells and modules

PILATUS

PILATUS - Deliverable report

D2.4 Specification of the M10 wafer line

Funded by the European Union

Deliverable No.	PILATUS D2.4	
Related WP	WP2	
Deliverable Title	Specification of the M10 wafer line	
Deliverable Date	23.10.2024	
Deliverable Type	REPORT	
Dissemination level	Public (PU)	
Author(s)	Brenda Malgapu (NOR) Arne Dahle (NOR)	
Checked by	Mathias Klinger (MBI)	2024-10-24
Reviewed by (if applicable)	Dirk Landgraf (MBG) Piter Miedema (UNR)	2024-10-28
Approved by	Anna Molinari (UNR) – Project coordinator	2024-10-29
Status	Final	2024-10-29

Document History:

Version	Date	Editing done by	Remarks
V1.0	23/10/2024	AD	first draft version, ready for review
V2.0	25/10/2024	AD	Revised version
V3.0	29/10/2024	AD	Revised version

Deliverable Background:

This report is part of the work package “Wafer and Cell Pilot line”, and therein related to the task “High quality M10 Wafer production”. This task addresses the specific ramp up of a M10 silicon-wafer production line by the project partner NorSun. The report describes the required changes and modifications, which are required to switch from the formerly used M6 wafer format (166 x 166 mm^2) to the larger M10 format (182 x 182 mm^2). It gives a comprehensive overview of the tool modifications for the i) Prewash, ii) Singulation, iii) Final Cleaning, and iv) Wafer Inspection. To ensure the desired quality of the wafers, an experimental plan is presented for each process step.

Contents

List of Figures

Abbreviations & Definitions

Abbreviation	Explanation
AOI	Automatic Optical Inspection
CDA	Compressed dry air
DI	De-ionized water
FC	Final cleaning
FMEA	Failure Mode and Effect Analysis
MSA	Measurement system analysis

1 Introduction

The silicon wafer is the centrepiece of a solar cell and the starting point for the production of a wafer is polysilicon. Polysilicon is filled into a quartz crucible which is inserted into a crystal puller. The polysilicon is melted in the furnace chamber and the melt is doped into n-type or p-type semiconductor. Next, a seed is inserted into the melt and a cylindrical single-crystalline ingot is pulled from the melt. For M10 wafers, the ingot has a growth diameter of 252 mm in order to provide a wafer diameter of 247 mm. In the shaping department, the top and tail are removed and also the 'wings', resulting in rectangular bricks, which are glued onto a sacrificial base plate on a work piece holder. In the next step, the assembly is inserted into multistrand diamond wire saws and thousands of wafers are sliced from the brick. Afterwards, the assembly is removed from the saw and the final step is the wafer line which is the topic of this report.

The current wafering equipment at NorSun is compatible with wafer sizes up to M6 format (flat-to-flat length of 166 mm and wafer diagonal of 228 mm). In order to accommodate for the increased wafer area of the M10 format (flat-to-flat length of 182 mm and wafer diagonal of 247 mm), see Figure 1, the existing wafering equipment needs to be adapted and modified.

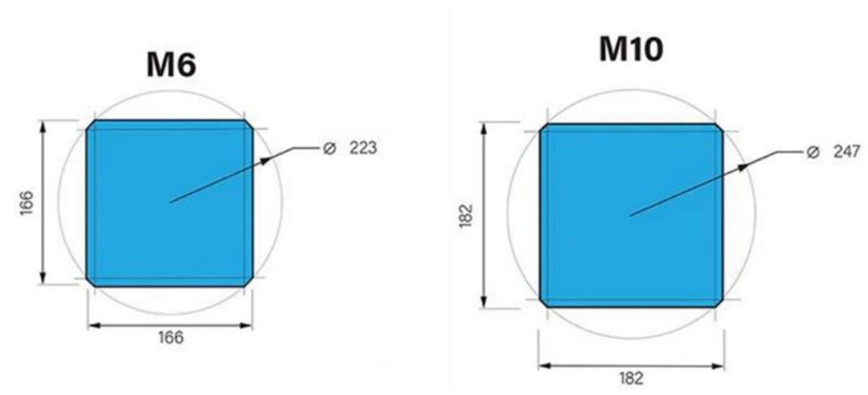

Figure 1: Comparison of M6 and M10 wafer formats (dimensions in mm).

1.1 Wafer cleaning process

As preparation for wafer slicing, monocrystalline silicon blocks are glued onto a sacrificial baseplate, which is glued to a work piece holder made of steel or aluminium, as depicted in Figure 2.

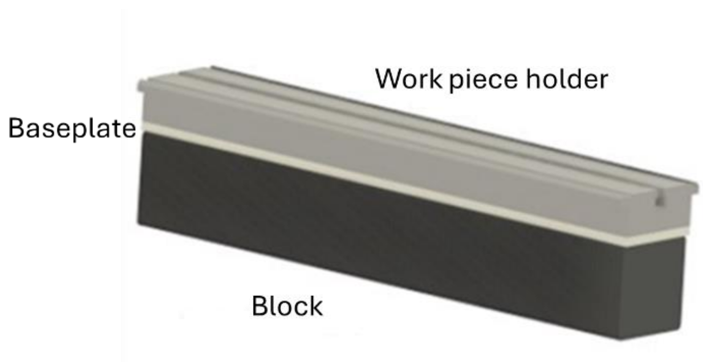

Figure 2: Schematic drawing of the slicing assembly: Monocrystalline silicon block glued on a baseplate, which is glued on a work piece holder

M10 blocks will be sliced using diamond wire sawing technology to produce M10 wafers with specified thickness. The sliced blocks will be transferred to the wafer cleaning equipment as shown in Figure 3.

Figure 3: After slicing the block will be unloaded from the wafer saw and lowered (yellow arrow) into a transfer cart filled with cutting fluid or process water.

The as-cut wafers are then separated and cleaned to remove contaminants on the wafer surface, followed by an automated optical inspection (AOI). All four wafer cleaning process steps (see also Figure 4) need to be adapted to the larger wafer format.

The overall physical and chemical principles of the wafer cleaning sub-processes will remain unchanged.

Figure 4: Wafer cleaning process steps: (i) Prewash, (ii) singulation, (iii) final cleaning, and (iv) automatic optical inspection (AOI)

1.2 Challenges for the wafer pilot line

NorSun's existing wafer cleaning equipment has been designed to handle wafer sizes up to M6 wafer format. Modification outside the design criteria poses challenges beyond the adaptation of wafer carriers and other wafer-handling components to the larger physical size of the wafers. This includes, but is not limited to:

- Increased risk of wafer breakage and chipping
- Reduced cleaning efficiency
- Adaptation of process times may lead to reduced tool capacities
- Reduced inspection efficiency (pixel size)

The necessary modifications to NorSun's wafer cleaning equipment are described in detail in section 2.1.

The main chapter 2 of this report describes the specification of the wafer line and the accompanying planned experiments. It is separated into section 2.1, where the necessary modifications to NorSun's wafer processing tools are described in detail and section 2.2. Section 2.1 includes the i) prewash, ii) singulation, iii) final cleaning, and iv) wafer inspection (cf. Figure 4). In section 2.2, the experimental plan and quality check is further detailed.

2 Specification on wafer line and experimental plan

The wafer cleaning equipment must be modified to accommodate the larger wafer size (M10), which will be described in section 2.1. Such modifications entail testing for form, fit and function to meet the process conditions before being used in mass production. M10 wafers processed by the modified tools shall be subjected to quality tests to verify compliance with customer requirements. This will be described in section 2.2.

2.1 Tool Modifications

2.1.1 Prewash

The prewash process intends to remove loose silicon-kerf generated by the slicing process from the wafer surfaces. The sliced silicon block is immersed in water and exposed to high pressure oscillating water spray jets from both sides as shown in Figures 5 and 6.

Figure 5: Schematic drawing of water spray nozzles during prewash (left) and spray jets during operation (middle and right)

When the block is placed inside the tank the spray nozzles are in home (OPEN) position. After the block is positioned correctly inside the tank, the side spray nozzles move to CLOSE position at a specified gap between the block and the nozzle. The spray is then activated alternately.

Figure 6: Picture of the spray nozzles of the prewash equipment

The spray nozzle positioning must be programmed to move at a distance to fit the M10 size. Some parts, such as the shaft also need to be modified to the changed geometry. The tank sizes of the precleaning equipment are sufficient to accommodate these upgrades.

As the penetration of the spray jets from the size will result in lower silicon kerf removal efficiency at the centre of the blocks, the spray sequence needs to be adjusted. In addition, the secondary purpose of the prewash, the de-gluing of the wafers from the baseplate using a bath of heated lactic acid, needs to be prolonged. Both effects will presumably reduce the capacity of the prewash tool upon adaptation from M6 to M10 wafer format.

2.1.2 Singulation

After the prewash cycle the de-glued baseplate and work piece holder is removed and the wafers are manually transferred to singulation wafer carriers that are stored in water. The size of the wafer carriers needs to be modified for use with M10 wafers, as indicated in Figure 7. Due to capillary forces the wafers stick together in the wafer carriers and need to be separated. The separation principle does not need to be changed upon transition from M6 to M10 wafers.

Figure 7: Singulation wafer carriers filled with M6 wafers (left) and comparison of existing carrier with M10 wafer size indicating the need for width adjustment

The singulation wafer carriers are loaded into the singulation tool where they are individually separated by water jets from both sides, picked up by transport belts, and aligned before loading into wafer cassettes. Due to the increased width of M10 wafers, nozzle positions, wafer aligner geometry, and cassette design must be modified. See also Figure 8.

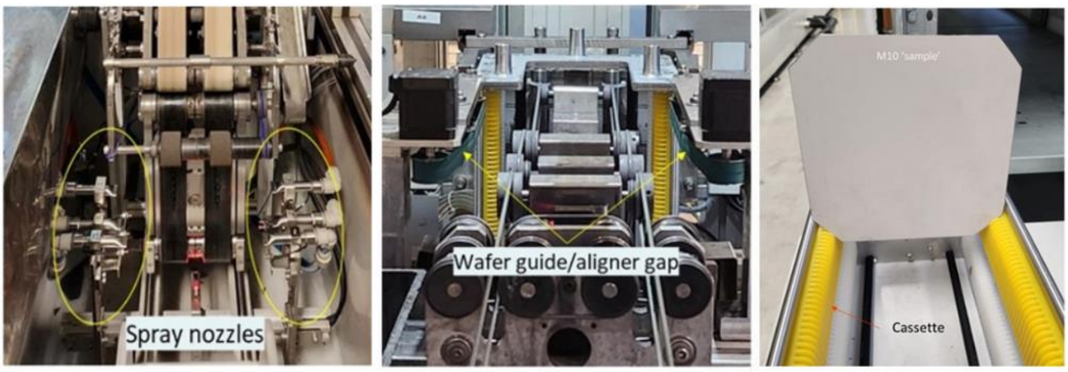

Figure 8. Images of spray nozzle positioning during wafer separation (left), wafer position aligner (middle), and comparison of M10 wafer size with M6 wafer cassette.

One of the most critical parts of the modification in the wafer line is the cassette redesign, which needs to ensure both handling of larger wafers as well as compliance with existing equipment dimensions. Some aspects of the cassette modifications are shown in Figures 9 to 11.

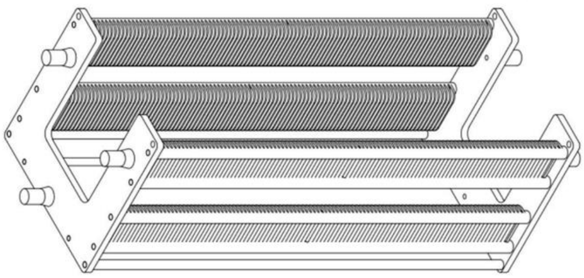

Figure 9: Generic design of wafer cassette for batch-wise cleaning

The wafer cassette is used for the batch-wise transfer of wafers through the different process baths of the wafer cleaning line. It consists of a frame and a slotted tooth plate to hold wafers, as indicated in Figure 9. In order to limit hardware adjustments of the existing wafer line, the frame design was chosen to accommodate the same number of cassettes per tank. However, the tooth plate distance needs to be adjusted to the increased flat-to-flat length of the M10 wafers, which resulted in extending the plate beyond the frame as indicate in Figure 10.

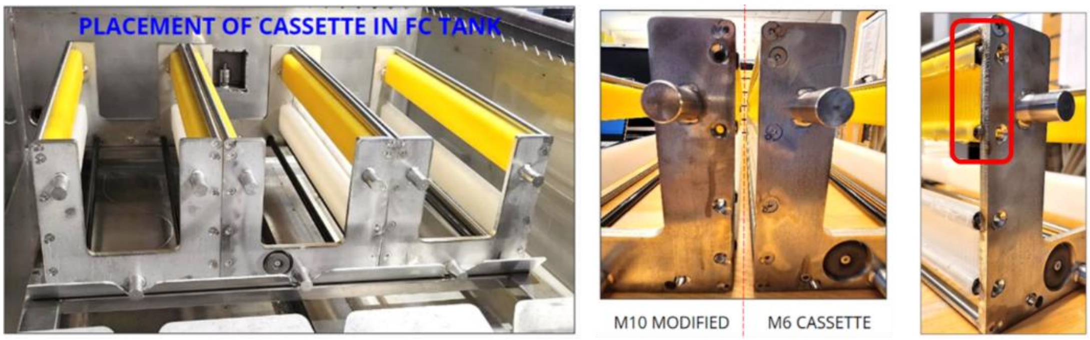

Figure 10: Placement of three cassettes side-by-side in the final cleaning (FC) line tank (left), comparison of the modified M10 and M6 cassettes (middle), and close up of the frame plate extending beyond the frame of the modified M10 cassette (right).

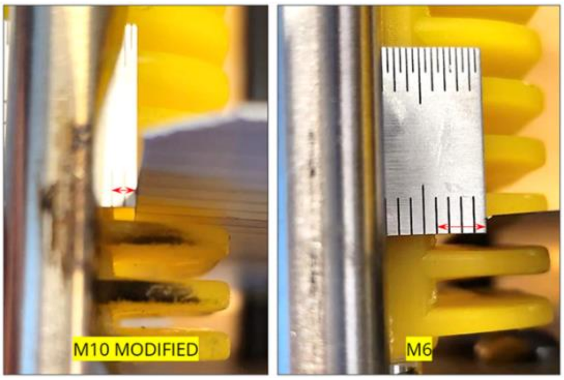

Figure 11: Comparison of the dimensional tolerance of the wafer edges for the modified M10 (left) and the original M6 (right) cassettes

Because of the larger distance between the tooth plates, the tolerance between the wafer edges and the cassette is reduced. This poses a risk for increased wafer chipping or breakage during loading and handling of the cassettes. The proper functioning of the wafer aligner will be of increased importance for M10 wafer cleaning in order to allow smooth wafer transport on each slot of the cassette.

Furthermore, the deflection of the wet M10 wafer in the cassette must also be considered to prevent wafer sticking (kissing wafer) which can cause breakages and pile-up during production. The bow of the wafer will increase from M6 to M10 format. For a dry wafer the deflection can be calculated using beam theory. A slot width of 4.76 mm, well below the expected wafer bow [1], will ensure that the risk of kissing wafers is reduced. Details on the effects of thinner and larger wafers are described in the deliverable report D2.2 (sensitive) of the Pilatus project.

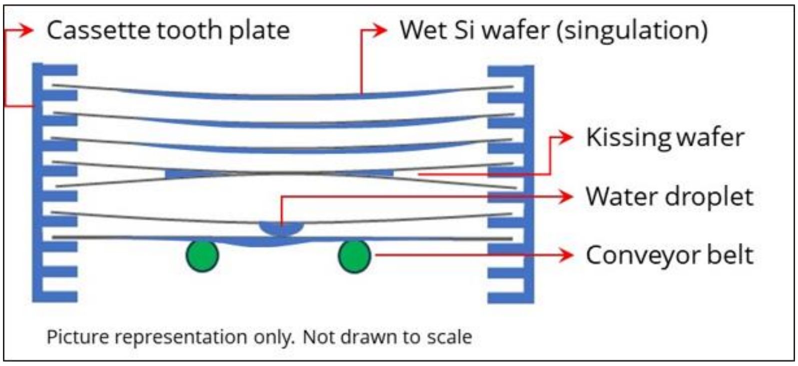

Figure 12: Schematic drawing of potential kissing wafer phenomenon during cassette loading.

To summarize, the following singulation items will be modified to accommodate for M10 wafer size:

- Carrier for stack of wafers for singulation
- Nozzle positioning and gap
- Wafer guide/aligner gap
- Cassette picker claw movement
- Cassette sensor repositioning
- Cassette (wafer carrier for final cleaning)

2.1.3 Final Cleaning

The cleaning process sequence (see Figure 13) will remain the same for M10 wafers as for M6 wafers. There will be a batch-wise transfer of the wafer cassettes. The cleaning process contains 15 steps including loading, pre-cleaning, cleaning, rinsing, organic cleaning, slow extraction, drying, buffering, and unloading to the wafer inspection unit.

		Wet part									Dry part				
	Loading	Pre-clean	Cleaning			Rinse	Org.Clean	Rinse		Slow extr.	Drying		Cooling/buff.		Unloading
Position	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Material		SUS316	SUS316	SUS316	SUS316	SUS316	PFA or PVDF	SUS316	SUS316	SUS316	SUS304	SUS304			
Step	DI-water spray	Ultrasonic	Ultrasonic	Ultrasonic	Ultrasonic	Ultrasonic		Ultrasonic	Ultrasonic	Extraction	Drying	Drying	Cooling / Buff	Cooling / Buff	
Process		DI-water	DI-water	DI-water	DI-water	DI-water	DI-water	DI-water	DI-water	DI-water	CDA	CDA	CDA	CDA	
Chemistry			Alkaline	Alkaline	Alkaline		H2O2 or O3								
Temp. Range		0 - 50°C	40 - 80°C	40 - 80°C	40 - 80°C	40 - 80°C	RT-70°C	RT - 50°C	RT - 50°C	RT - 85°C	RT - 95°C	RT- 95°C	RT	RT	

Figure 13: Summary of wafer line baths and process steps

Only minor changes will be done on the final cleaning (FC) tool as the tank sizes are large enough to hold the modified M10 wafer carriers. FC tool will require modification of the cassette picker, the positioning of the cassette unloading sensor, the transfer unit lifter plates (Figure 14), cassette aligners (Figure 15), and the cassette return belt (Figure 16).

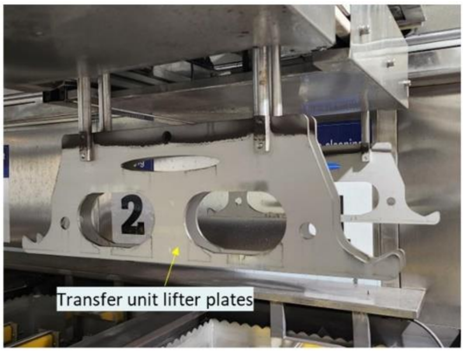

Figure 14: Image of the transfer unit lifter plates of the final cleaning line

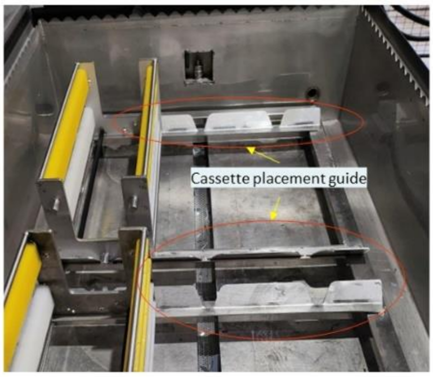

Figure 15: Image of the cassette placement guides inside the tanks of the final cleaning unit

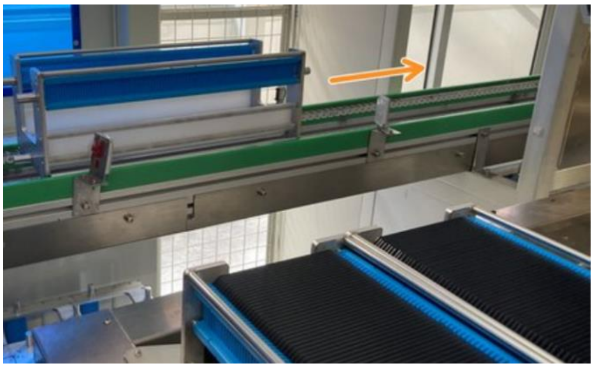

Figure 16: Return belt for transfer of wafer cassettes from unloading to loading

To summarize, the following FC items will be modified to accommodate for M10 wafer size:

- Cassette modification
- Cassette picker
- Cassette unloading sensor
- Cassette placement guides
- Transfer unit lifter plates
- Cassette return belt

2.1.4 Wafer Inspection

In order to capture the larger wafer area and wafer edges, the camera positions, calibrations, and analysis software of the automatic optical inspection (AOI) tool (see Figure 17) need to be adapted to M10 wafer format. Software debugging, reprogramming, and hardware alignment will be done by the vendor. The height of the camera for inspection will be adjusted to capture the full M10 wafer size (field-of-view).

Figure 17: Image of automatic optical wafer inspection unit (Source: Applied Materials [2])

The following AOI items will be modified to accommodate for M10 wafer size:

- Cassette loader
- Wafer aligner distance
- Geometry camera position (see Figure 18)
- Side chip camera positions (see Figure 19)

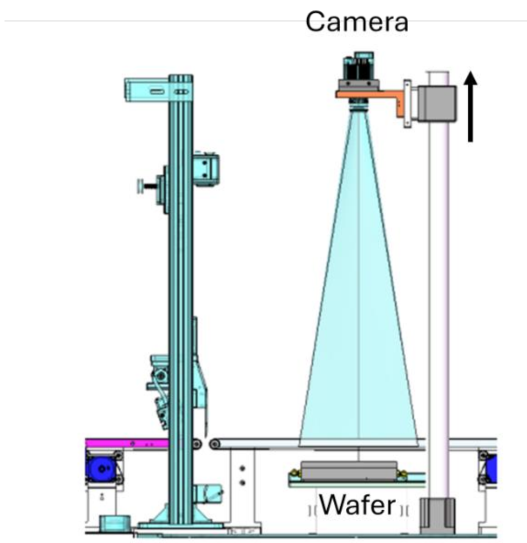

Figure 18: Schematic drawing of set-up for wafer geometry measurements. The camera position needs to be adjusted to capture the increased wafer area.

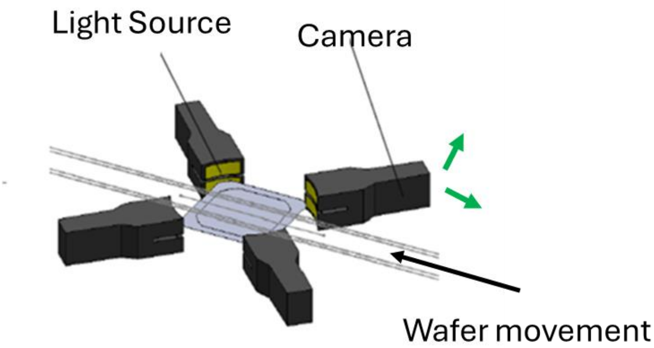

Figure 19: Schematic drawing side chip detection (adapted from Applied Materials)

2.2 Experimental plan and quality check

The modification of existing wafer cleaning tools poses the risk of reduced production yields as a result of increased breakages, chipping, double wafers, or reduced cleaning efficiency due to increased silicon kerf loads. Furthermore, over- and/or under-rejection of wafer defects during inspection needs to be prevented after AOI adaptation to M10 format. Detailed testing and verification (see also Figure 20) will be done to confirm the suitability of the wafer line modifications for mass production of M10 wafers.

- Functionality tests will be conducted on all modified equipment (to check for tool limitations and other issues that may occur during production) to ensure smooth operations.
- Dummy runs will be done and quality tests on wafers such as Four-Point-Bending test will be performed on wafers to check for wafer strength before and after each process step.
- Etching wafers after the cleaning process will be performed to check for wafer cleaning efficiency and guarantee good surface quality to customers.
- Wafer and bath solution samples will be sent for metals analysis to verify that the wafer line process does not introduce other contaminants on its product that will affect customer satisfaction.
- Weekly Measurement System Analysis (MSA) will be conducted to ensure accuracy and repeatability of measurements and detection of the wafer inspection tool.

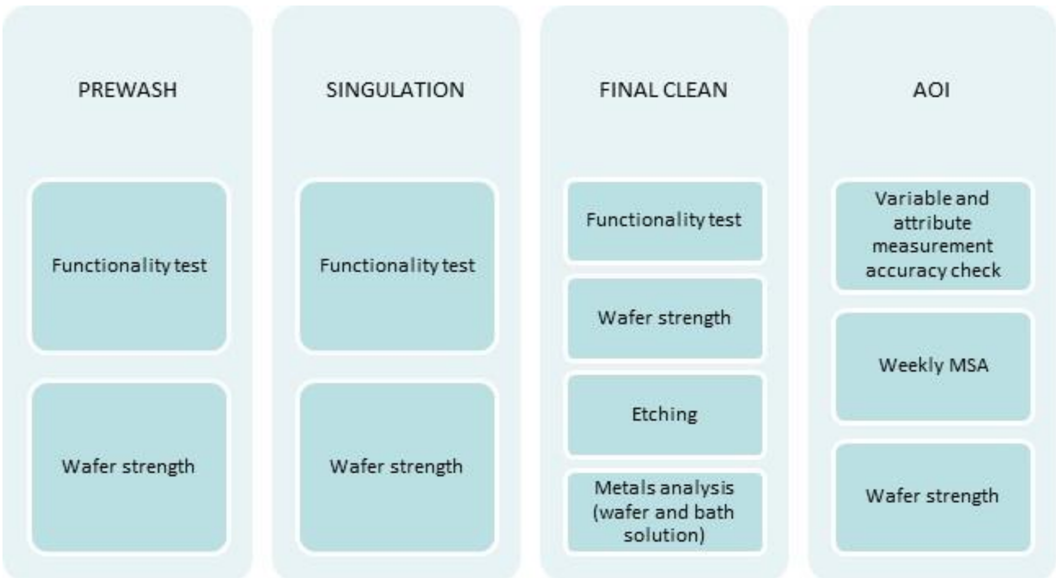

Figure 20: Overview of tests and verifications for the M10 modifications of the wafer line

3 Conclusion

Detailed assessment has been done to determine the adjustments and upgrades required to convert the existing M6 wafer line at Norsun to be capable of handling M10 wafers. In this report, a summary on the development of new equipment design and modification is given. A detailed Failure Mode and Effect Analysis (FMEA) has been completed and all potential failure modes have been managed. Overall, the wafer line with the suggested modifications should be capable of handling M10 format wafers.

4 References

[1] PILATUS – Deliverable report D2.2 Thin wafer approach for the cell pilot line

[2] https://www.appliedmaterials.com/sg/en/product-library/applied-vericell-solar-wafer-inspection-system.html (retrieved 25/10/24)

5 Risks and interconnections

5.1 Risks/problems encountered

Risk No.	What is the risk	Probability of risk occurrence[1]	Effect of risk[1]	Solutions to overcome the risk
9	Wafering line not ready in time	Medium	Low	Buying more benchmark wafers from other existing M10-wafer suppliers until M10 from Norsun is available.
U1	M10 wafer line may not be build with all its requirements, because Chinese suppliers will not deliver key components	Low	High	One option is to order tools as soon as possible from China (with the attempt to be earlier then the restriction /prohibitions by the Chinese government taking effect). The rest risk is that the delivered equipment can likely not be serviced by the Chinese suppliers afterwards. If NOR is not able (not in time, not willing to have no servicing options) to order tools and equipment from China, then there are two mitigation strategies: i) Make use of the existing equipment and tool set at NOR, which is originally not designed for M10, but preliminary these are shown to work for 9" (M6) wafers. 10" (M10) will be tight but could be possible. Setting up a project to investigate this matter in more detail is an option. ii) Make use of a supplier outside of China (for example there is a supplier in Germany which has equipment (which is more sophisticated and meant for semiconductor technology) that would fit the needs for PILATUS but has to be stripped / adjusted. Disadvantage is that this will not be a mainstream solution that NOR can go forward with for later upscaling and the prizes are higher.
U13	The ramp-up of the M10 silicon wafer pilot line planned for NCR in T2.3 cannot be achieved, leading to jeopardising of the achievement of one	Medium	Medium	Meyer Burger confirms that the targets on the cells and modules pilot lines will still be achieved by using M6 wafers and/or importing M10 wafers from China. However, the consortium is still aiming to demonstrate and provide within PILATUS a "full European value chain" from wafer to module production, so a new wafer producer should be involved in the project. After addition of NOR update: allowing NOR to ramp-up their M10

	of the project targets			wafer line as much as possible in the remaining time of the project.

1) Probability risk will occur: 1 = high, 2 = medium, 3 = Low

5.2 Interconnections with other deliverables

Efficiency of solar cells with wafers with <130 µm thickness to be reported in D2.5 will depend on the production of thin M10 wafers.

6 Deviations from Annex 1

Compared to the original Annex 1 (before the amendment), there was a delay in the M10 wafer line specification. After the first amendment and NOR's entry in the PILATUS consortium in M14, the development of M10 pilot production design started.

7 Acknowledgement

The author(s) would like to thank the partners in the project for their valuable comments on previous drafts and for performing the review.

Project partners:

#	Partner short name	Partner Full Name
1	UNR	Uniresearch BV
2	MBG	Meyer Burger (Germany) GmbH
3	MBI	Meyer Burger (Industries) GmbH
4	FhG	Fraunhofer Gesellschaft zur Forderung der Angewandten Forschung EV
5	FZU	Fyzikalni Ustav AV CR V.V.I
6	EURAC	Accademia Europea di Bolzano
7	EXATEQ	Exateq GmbH
8	TNO	Nederlandse Organisatie Voor Toegepast Natuurwetenschappelijk Onderzoek TNO
9	NCR	Norwegian Crystals AS (terminated)
10	ULIEGE	Universite de Liege
11	PADA	Finproject SpA
12	ISRA	ISRA VISION GmbH
13	CSEM	CSEM Centre Suisse d'Eletronique et de Microtechnique SA – Recherche et Developpement
14	MBCH	Meyer Burger AG
15	MBR	Meyer Burger Research AG
16	PASAN	PASAN SA
17	WCH	Wacker Chemie AG
18	EPFL	École Polytechnique Fédérale de Lausanne
19	CPT	Cambridge Photon Technology Limited
20	NOR	Norsun AS

Disclaimer/ Acknowledgment

This project has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement No 101084046. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union. Neither the European Union nor the granting authority can be held responsible for them.